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10/692,800	10/27/2003	Hideo Miyake	1450.1005D	1082

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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,800	MIYAKE ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/27/2008 has been entered.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 14-20, 33, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Alpert et al., U.S. Patent No. 5,740,413 (Hereinafter Alpert).

3. Referring to claim 14, Alpert has taught an interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said apparatus comprising:

a break detection section for detecting a breakpoint set at an arbitrary position of an instruction sequence *[detecting a branch instruction when the branch breakpoints are enabled; column 6, lines 38-55]*;

a condition determination section for determining whether an instruction of a designated address is executed as satisfying a branch condition of said conditional instruction *[determining if the branch is taken; column 6, lines 38-55]*; and

a control section for controlling a break-interrupt based upon of a breakpoint detection result from said break detection section and execution of the instruction of the designated address according to a branch condition determination result from said condition determination section *[a breakpoint is generated if a branch is taken and branch breakpoints are enabled; column 6, lines 38-55]*.

4. Referring to claim 15, Alpert has taught an interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said apparatus comprising:

an instruction break detection section for detecting an instruction break in accordance with whether an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read, and outputting a detection signal representing a detection result *[detecting a breakpoint using the address breakpoint unit; column 6, line 63 – column 7, line 10]*;

a condition determination section for determining whether an instruction of a designated address is executed as satisfying a branch condition the conditional instruction, and outputting a branch condition determination signal *[the branch breakpoint unit sends a signal in response to determining that branch is or will be taken; column 6, lines 38-55]*; and

a logical operation section for performing AND operation to said detection signal output from said instruction break detection section and execution of the instruction of the designated address according to said branch condition determination signal output from said condition determination section, and sending a break-interrupt notification in accordance with the AND operation result *[the debug circuitry generates a breakpoint in accordance with the address breakpoint unit and branch breakpoint unit; column 6, lines 20-31]*.

5. Referring to claim 16, Alpert has taught an apparatus according to claim 15, wherein

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal *[column 6, lines 38-55]*, and

when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied branch condition, said logical operation section sends said break-interrupt notification *[column 6, lines 38-55]*.

6. Referring to claim 17, Alpert has taught an apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied *[enabling/disabling the enable bit for the branch breakpoint unit changes between a modes that generates a breakpoint on a taken branch and one that doesn't; column 6, lines 20-31]*,

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal *[column 6, lines 38-55]*, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, said logical operation section does not sends the break-interrupt notification, and when said instruction word is the conditional instruction having a satisfied branch condition, said logical operation section sends the break-interrupt notification, and in said second mode, when said instruction word is an

instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification *[column 6, lines 20-31]*.

7. Referring to claim 18, Alpert has taught an apparatus according to claim 15, wherein

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal *[column 6, lines 38-55]*, and

when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied branch condition, said logical operation section sends said break-interrupt notification *[column 6, lines 38-55]*.

8. Referring to claim 19, Alpert has taught an apparatus according to claim 15, wherein

said apparatus further comprises a mode setting section for setting one of a first mode in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the branch condition of said conditional instruction is satisfied, and a second mode in which said break-interrupt is generated when said generation condition of said instruction break is satisfied *[enabling/disabling the enable bit for the branch breakpoint unit changes between a modes that generates a breakpoint on a taken branch and one that doesn't; column 6, lines 20-31]*,

said condition determination section is designed to determine whether an instruction word is said conditional instruction, if said instruction word is said conditional instruction, determine whether the branch condition of the conditional instruction is satisfied, and output the branch condition determination signal *[column 6, lines 38-55]*, and

in said first mode, when an instruction word corresponding to the instruction address representing said breakpoint is a conditional instruction having an unsatisfied branch condition, said logical operation section does not send the break-interrupt notification, and when said instruction word is an unconditional instruction or the conditional instruction having a satisfied branch condition, said logical operation section

sends the break-interrupt notification, and in said second mode, when said instruction word is an instruction word corresponding to the instruction address representing said breakpoint, said logical operation section sends said break-interrupt notification *[column 6, lines 20-31]*.

9. Referring to claim 20, Alpert has taught an apparatus according to claim 15, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction, a long instruction word processor for parallel executing short instructions forming a long instruction word, and a parallel processor for parallel executing at least one basic instruction forming a variable-length instruction word *[column 5, lines 14-16]*.

10. Referring to claim 33, Alpert has taught an interrupt control method for controlling a break-interrupt in a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition of the conditional instruction is satisfied are indivisible, said method comprising the steps of:

detecting a breakpoint set at an arbitrary position of an instruction sequence *[detecting a branch instruction when the branch breakpoints are enabled; column 6, lines 38-55]*;

determining whether an instruction of a designated address is executed as satisfying a branch condition said conditional instruction *[determining if the branch is taken; column 6, lines 38-55]*; and

controlling the break-interrupt based upon the detecting of said breakpoint and execution of the instruction of the designated address according to the determining of the branch condition of said conditional instruction *[a breakpoint is generated if a branch is taken and branch breakpoints are enabled; column 6, lines 38-55]*.

11. Referring to claim 34, Alpert has taught an apparatus comprising:

A controller *[branch breakpoint unit; FIG. 1, component 190]*

detecting a breakpoint set at an arbitrary position of an instruction sequence *[detecting a branch instruction when the branch breakpoints are enabled; column 6, lines 38-55]*;

determining execution of an instruction of a designated address as satisfying a branch of an instruction *[determining if the branch is taken; column 6, lines 38-55]*; and

controlling a break-interrupt based upon the detecting the breakpoint and the execution of the instruction of the designated address by the determining of the branch of the instruction, according to a logical operation of a detection signal from said breakpoint detection and a branch condition determination signal from said branch control determination of the instruction *[the branch breakpoint unit determines if a branch is taken and branch breakpoints are enabled; column 6, lines 38-55]*; and

sending a break-interrupt notification in accordance with the logical operation *[a breakpoint is generated if a branch is taken and branch breakpoints are enabled; column 6, lines 38-55]*.

12. Claims 21-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Alverson et al., U.S. Patent No. 6,480,818 (Herein referred to as Alverson).

13. Referring to claim 21, Alverson has taught an interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition is satisfied are indivisible, said apparatus comprising:

an instruction break detection section *(target thread execution subroutine; Fig. 11, component 1100)* for detecting an instruction break in accordance with whether an instruction corresponding to an instruction address representing a breakpoint, which is set in a register, is read *[The break instruction, which corresponds to an address and is set in a register (See Fig. 4B), is inherently read out for instruction execution]*, and sending a break-interrupt notification in accordance with the detecting of the instruction break *[The target thread execution subroutine detects an instruction break (i.e. breakpoint; See Fig. 11, component 1110) and notifies the breakpoint handler subroutine (i.e. sends a break-interrupt notification); See column 21, lines 15-39 and Fig. 11]*; and

a control section *(breakpoint handler subroutine; Fig. 12, component 1125)* for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said instruction break detection section *(target thread execution subroutine)*, determining whether an instruction of a designated address is executed as satisfying a branch condition of said conditional instruction is satisfied, and controlling break-interrupt processing in accordance with the determining of execution of the instruction of the designated address as satisfying the branch condition of the conditional instruction *[The breakpoint handler subroutine determines if a condition of the conditional instruction is satisfied (and, therefore, the breakpoint is valid) and notifies the nub (i.e. controls break-interrupt processing) if the condition is satisfied; See column 21, lines 51-66]*.

14. Referring to claim 22, Alverson has taught an apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction *(The breakpoint handler subroutine determines if whether or not the breakpoint instruction is conditional; See Fig. 12, component 1210)*, and when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied *(See Fig. 12, component 1225)*, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler *(The breakpoint handler subroutine always eventually returns; See last step of Fig. 12)*, and when said instruction word as said instruction break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing *[When the condition is satisfied (i.e. true) the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*.

15. Referring to claims 23 and 29, taking claim 23 as exemplary, Alverson has taught an apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section *(nub thread execution routine; Fig. 5, component 500)* for setting one of a first mode *(mode when breakpoint set is a conditional breakpoint)* in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of the branch of said conditional instruction is satisfied, and a second mode *(mode*

when breakpoint set is an unconditional breakpoint) in which said break-interrupt is generated when said generation condition of said instruction break is satisfied *[The nub thread execution routine sets a breakpoint mode by recording information indicating whether the inserted breakpoint is conditional or not; column 15, lines 43-63]*, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction *(See Fig. 12, component 1210)*, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied *(See Fig. 12, component 1225)*, when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler *(The breakpoint handler subroutine always eventually returns; See last step of Fig. 12)*, and when said instruction word as said instruction break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing *[When the condition is satisfied (i.e. true) the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*, and

in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification *[In the second mode the breakpoint set is unconditional and, therefore, the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*.

16. Referring to claims 24 and 30, taking claim 24 as exemplary, Alverson has taught an apparatus according to claim 21, wherein said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction *(The breakpoint handler subroutine determines if whether or not the breakpoint instruction is conditional; See Fig. 12, component 1210)*, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied *(See Fig. 12, component 1225)*, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler *(The breakpoint handler subroutine always eventually returns; See last*

step of Fig. 12), and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing *[When the breakpoint is unconditional or conditional and the condition is satisfied (i.e. true) the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*.

17. Referring to claims 25 and 31, taking claim 25 as exemplary, Alverson has taught an apparatus according to claim 21, wherein

said apparatus further comprises a mode setting section *(nub thread execution routine; Fig. 5, component 500)* for setting one of a first mode *(mode when breakpoint set is a conditional breakpoint)* in which said break-interrupt is generated when a generation condition of said instruction break is satisfied, and the condition of the branch of said conditional instruction is satisfied, and a second mode *(mode when breakpoint set is an unconditional breakpoint)* in which said break-interrupt is generated when said generation condition of said instruction break is satisfied *[The nub thread execution routine sets a breakpoint mode by recording information indicating whether the inserted breakpoint is conditional or not; column 15, lines 43-63]*, and

in said first mode, said control section determines, in said interrupt handler, whether an instruction word as an instruction break target is said conditional instruction *(See Fig. 12, component 1210)*, when said instruction word is said conditional instruction, determines whether the condition of the branch of said conditional instruction is satisfied *(See Fig. 12, component 1225)*, when said instruction word as said instruction break target is a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler *(The breakpoint handler subroutine always eventually returns; See last step of Fig. 12)*, and when said instruction word as said instruction break target is an unconditional instruction or a conditional instruction having a satisfied branch condition, performs said break-interrupt processing *[When the condition is satisfied (i.e. true) or breakpoint is unconditional the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*, and

in said second mode, said control section performs said break-interrupt processing when receiving said break-interrupt notification *[In the second mode the breakpoint set is unconditional and, therefore, the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*.

18. Referring to claims 26 and 32, taking claim 26 as exemplary, Alverson has taught an apparatus according to claim 21, wherein said data processing system comprises one of a scalar processor for performing one unit of processing in accordance with one instruction *(See Fig. 3, component 101 and column 1, lines 20-40)*, a long instruction word processor for parallel executing short instructions forming a long instruction word, and a parallel processor for parallel executing at least one basic instruction forming a variable-length instruction word.

19. Referring to claim 27, Alverson has taught an interrupt control apparatus applied to a data processing system having a function of executing a conditional instruction that executes a designated data processing when a designated branch condition of the conditional instruction is satisfied, wherein a determination of the branch condition of the conditional instruction and the executed data processing when the branch condition is satisfied are indivisible, said apparatus comprising:

a software break detection section *(target thread execution subroutine; Fig. 11, component 1100)* for detecting a software break in accordance with whether a breakpoint instruction placed at an arbitrary position of an instruction sequence is executed *(See Fig. 4)*, and sending a break-interrupt notification in accordance with the detection of the software break *[The target thread execution subroutine detects a software break (i.e. breakpoint; See Fig. 11, component 1110) and notifies the breakpoint handler subroutine (i.e. sends a break-interrupt notification); See column 21, lines 15-39 and Fig. 11]*; and

a control section *(breakpoint handler subroutine; Fig. 12, component 1125)* for, in an interrupt handler activated in accordance with said break-interrupt notification supplied from said software break detection section *(target thread execution subroutine)*, determining whether an instruction of a designated address is executed as satisfying a branch condition of said conditional instruction, and controlling break-interrupt processing in accordance with the determining of execution of the instruction of the designated address as satisfying the branch condition of the conditional instruction *[The breakpoint handler*

subroutine determines if a condition of the conditional instruction is satisfied (and, therefore, the breakpoint is valid) and notifies the nub (i.e. controls break-interrupt processing) if the condition is satisfied; See column 21, lines 51-66].

20. Referring to claim 28, Alverson has taught an apparatus according to claim 27, wherein said control section determines, in said interrupt handler, whether an instruction word as a software break target is said conditional instruction *(The breakpoint handler subroutine determines if whether or not the breakpoint instruction is conditional; See Fig. 12, component 1210)*, and when said instruction word is said conditional instruction, determines whether the branch condition of said conditional instruction is satisfied *(See Fig. 12, component 1225)*, and when said instruction word as said software break target is an unconditional instruction or a conditional instruction having an unsatisfied branch condition, returns from said interrupt handler *(The breakpoint handler subroutine always eventually returns; See last step of Fig. 12)*, and when said instruction word as said software break target is a conditional instruction having a satisfied branch condition, performs said break-interrupt processing *[When the condition is satisfied (i.e. true) the breakpoint handler subroutine notifies the nub (See Fig. 12, component 1240), which performs break-interrupt processing; See column 22, lines 45-65]*.

Response to Arguments

21. Applicant's arguments filed 05/27/2008 have been fully considered but they are not persuasive.

22. The applicant argues the novelty/rejection of the claims, in substance that:

> "Neither Alpert et al. (USP 5,740,413) nor Alverson et al. (USP 6,480,818) disclose, either expressly or inherently, that a break-interrupt is generated when an instruction for execution is an instruction of a designated address (conditional instruction) and the condition of the conditional instruction is satisfied, as in the present invention, namely 'a condition determination section for determining whether an instruction of a designated address is executed as satisfying a branch condition of said conditional instruction ~~is satisfied~~; and a control section for controlling a break-interrupt based upon a breakpoint detection result from said break detection section and execution of the instruction of the designated address according to a branch condition determination result from said condition determination section" (page 11)

23. These arguments are not found persuasive for the following reasons:

The applicant states that "in Alpert the processor generates a break each time an instruction that causes a branch to be taken is executed". The examiner agrees with this statement. That is, Alpert has

taught that, when the branch breakpoint unit is enabled, the branch breakpoint unit controls a break-interrupt by determining whether a branch instruction (i.e. an instruction of a designated address) is executed as satisfying a branch condition (i.e. results in a taken branch) [Alpert; column 6, lines 38-55]. It appears to the examiner that the applicant is reading the limitation regarding the condition determination section too narrowly. Specifically, it appears that the applicant is reading the limitation "an instruction of a designated address" as indicating the recited instruction is an instruction located at an address specified as a breakpoint address. However, the limitation as claimed does not require such a reading. If the applicant intends for the claimed "instruction of a designated address" to be an instruction located at an address specified as a breakpoint address then the limitation should be amended appropriately.

Applicant argues that Alverson's conditional breakpoint ”merely refers to whether the nub has designated the breakpoint as valid or invalid”. Alverson uses the terms "valid" and "invalid" to describe the result of the condition of a conditional branch instruction [Alverson; column 21, lines 51-66]. The determination of whether a breakpoint is valid or invalid is "determining whether an instruction of a designated address [i.e. the conditional branch instruction] is executed as satisfying a branch condition of said conditional instruction [i.e. whether the condition of the conditional branch instruction is valid]" as claimed. It appears to the examiner that the applicant is reading the limitation regarding the control section too narrowly. Specifically, it appears that the applicant is reading the limitation "an instruction of a designated address" as indicating the recited instruction is an instruction located at an address specified as a breakpoint address. However, the limitation as claimed does not require such a reading. If the applicant intends for the claimed "instruction of a designated address" to be an instruction located at an address specified as a breakpoint address then the limitation should be amended appropriately.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BPG/ 07/21/2008

Benjamin P Geib
Examiner
Art Unit 2181

/Tonia LM Dollinger/

Primary Examiner, Art Unit 2181